ABSTRACT

A new method and apparatus to verify the performance of a built-in self-test circuit for testing embedded memory in an integrated circuit device is achieved. A set of faults is introduced into an embedded memory behavior model. The embedded memory behavior model comprises a high-level language model. Each member of the set of faults comprises a finite state machine state, a memory address, and a memory data fault. The built-in self-test circuit and the embedded memory behavior model are then simulated. The built-in self-test circuit generates input data and address patterns for the embedded memory behavior model. The embedded memory behavior model outputs memory address and data in response to the input data and address patterns. The input address and data and the memory address and data are compared in the built-in self-test circuit and a fault output is generated if not matching. The fault output and the set of faults are compared to verify the performance of the built-in self-test circuit.